PATENT

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IN THE CLAIMS:

Please find below a listing of all of the pending claims. The statuses of the claims are set forth in parentheses.

1. (Original) An on-chip capacitor comprising:

a first electrode formed during a first deposition of a first metal layer of a multi-level semiconductor device;

a substantially thin dielectric layer configured to be deposited over said first electrode; and

a second electrode formed during a second deposition of a second metal layer of said multi-level deposition device, wherein said second electrode is formed over said substantially thin dielectric layer, wherein said on-chip capacitor is formed in a crossover area of said first metal layer and said second metal layer of said multi-level semiconductor device.

2. (Original) The on-chip capacitor according to claim 1, wherein an angle of intersection between said first metal layer and said second metal layer is between zero and ninety degrees.

3. (Original) The on-chip capacitor according to claim 1, wherein said first electrode and said second electrode are configured to be substantially parallel.

4. (Original) The on-chip capacitor according to claim 3, wherein said first electrode and said second electrode are further configured to be overlapping.

5. (Original) The on-chip capacitor according to claim 1, wherein said first electrode and said second electrode are configured as a rectangular planar structure.

6. (Original) The on-chip capacitor according to claim 5, wherein said first electrode and said second electrode are substantially parallel and overlapping.

7. (Original) The on-chip capacitor according to claim 1, wherein said substantially thin dielectric material comprises a composite of materials.

8. (Original) The on-chip capacitor according to claim 7, wherein said composite of materials includes PZT and platinum.

9. (Original) The on-chip bypass capacitor according to claim 1, wherein a dielectric constant of said substantially thin dielectric material layer is substantially high.

10. (Original) The on-chip bypass capacitor according to claim 9, wherein said substantially thin dielectric material layer includes silicon nitride.

11. (Original) The on-chip bypass capacitor according to claim 10, wherein said thickness of said substantially thin dielectric material layer is between 50 to 100 angstroms.